



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants : Kelly T. Hurley et al

Serial No. : 09/808,484

Confirm. No. : 3606

Filed : March 14, 2001

Title : **SELF-ALIGNED FLOATING GATE FLASH CELL SYSTEM  
AND METHOD**

Docket : : MIO 0064 PA

Examiner : Quinto, Kevin V.

Art Unit : 2826

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

**DECLARATION OF KELLY T. HURLEY, AND GRAHAM WOLSTENHOLME**  
**UNDER 37 C.F.R. 1.131**

Kelly T. Hurley, and Graham Wolstenholme, the applicants in the above-identified patent application, declare as follows:

1. We are the co-inventors of the subject matter of claims 12, 19, 20, 21, 22, 24, 25, 33, 34, 36-38, 40, 73, 74 and 76 of the above-identified patent application.
2. The above-identified application is assigned to Micron Technology, Inc., with whom we were employed on the filing date of this application.
3. We are familiar with the Office Action mailed March 31, 2003, including the rejections made by the Examiner therein. We are also familiar with the references cited by the Examiner in that Office Action, including the Shimizu et al (US 6,462,373) patent.
4. On a date prior to November 30, 2000, the filing date of the Shimizu et al patent, we had jointly conceived the subject matter of claims 12, 19, 20, 21, 22, 24, 25,

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33, 34, 36-38, 40, 73, 74 and 76 of this patent application. All of the acts reported below were carried out in the United States. As evidence to establish conception of the invention prior to the effective date of the reference coupled with due diligence from prior to said date to the filing of the application, we submit the following exhibits. As permitted by present practice, the date of each exhibit has been obscured.

a) Exhibit A is a photocopy of our invention disclosure showing conception of the claimed invention prior to November 30, 2000.

b) Exhibit B is a photocopy of a letter dated October 2, 2000 from outside patent counsel providing a first draft of a patent application covering the claimed invention prior to November 30, 2000, which shows due diligence prior to the effective date of the reference.

c) Exhibit C is a photocopy of a letter dated November 15, 2000 from our patent department regarding the first draft of the patent application covering the claimed invention prior to November 30, 2000, which shows continued due diligence prior to the effective date of the reference.

d) Exhibit D is a photocopy of a letter dated December 18, 2000 from outside patent counsel providing a revised draft of the patent application covering the claimed invention, which shows continued diligence to the filing of the application.

e) Exhibit E is a photocopy of a facsimile dated March 13, 2001 providing final comments from our patent department regarding the revised draft of the patent application, which shows continued diligence to the filing of the application.

5. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful and false statements and the like so made are punishable by fine or imprisonment, or both, under

Serial No.: 09/808,484  
Docket No.: MIO0064PA

Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application and any patent issued thereon.

Date: 6/26/03

Kelly T. Hurley  
Kelly T. Hurley

Date: ~~6/31/05~~ 7/1/03 Gaw

Graham Wolstenholme  
Graham Wolstenholme

**Micron Technology, Inc.**  
Invention Disclosure

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00-0028

If this disclosure is related to an ARPA project, please check one of the following:

☐ Advanced SRAM    ☐ BST    ☐ FED    ☐ FE RAM    ☐ NCAICM

1) **INVENTOR(s):**    Graham Wolstenholme  
                                 Kelly T. Hurley

If an inventor is NOT employed by Micron identify the inventor and employer:

2) **DESCRIPTION OF THE INVENTION:**

2.1    **Title of Invention:**

Simple Self Aligned Floating Gate Flash Cell

2.2    **Brief Description of Invention:**

Self Aligned Floating Gate (SA-FG) Flash Cell processes with increased capacitive coupling and no Floating Gate Photo steps.

2.3    **Attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.**

In a Flash memory process, the Floating Gate (FG) Photo step attempts to print the smallest space possible (0.155um 49 ACI CD target on our W33A in Fab3, a 0.22um design rule process) to maximize the FG Poly "wing" overlapping Fld Ox; this helps maximize the capacitive coupling of the cell.

The SA-FG process helps shrink the Flash cell (with a FG Poly 2 dep to create the wing) but the minimum Photo space possible is not scaling as fast as the rest of cell. Several papers have reported using a hard mask & spacer mask process before etching the FG Poly (Toshiba.)

Our disclosure presents several options to increase the coupling of the SA-FG Flash cell while completely eliminating the FG Photo step. The space between Floating Gates and the increased coupling is determined by the Isolation Space and the thicknesses of the thin films. (See the attached spreadsheet, and the diagrams for each option.)

option 1

1. SA-FG process thru STI CMP.
2. \* Fld Oxide etch back.
3. nitride removal.
4. \* FG Poly 2 dep.
5. \* "spacer" etch the FG Poly 2 leaving FG "wings" over the Fld Ox to increase coupling.
6. standard processing (ONO, CG Poly dep, CG Poly photo & etch, etc.)

option 2

1. SA-FG process thru STI CMP & nitride removal.
2. \* FG Poly 2 dep.
3. \* "spacer" etch the FG Poly 2 leaving FG "bat ears" (single-sided) up the sides of the Fld Ox to increase coupling.

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4. standard processing.

option 3

1. SA-FG process thru STI CMP & nitride removal.

2. \* FG Poly 2 dep

3. \* "spacer" etch the FG Poly 2 leaving FG "bat ears" up the sides of the Fld Ox to increase capacitive coupling.

4. \* Fld Oxide etch back (double-sided bat ears.)

5. standard processing.

### 3) **INFORMATION CONCERNING CONCEPTION OF INVENTION:**

#### 3.1 Conception and Documentation of the Invention:

- a. Identify the date when you first conceived the invention.  
(If not sure, give the earliest date of which you are sure)  
Nov. 30, 19 .
- b. To whom was the idea first described and on what date?  
(Other than co-inventor)  
Kirk Prall on Nov. 30, 19
- c. Identify the date of the first tangible record such as computer simulation, tape out, drawing, or written description. Please type and location.  
Notes & drawings in Kelly Hurley's notebook, Nov. 30, 19

3.2 Conception of the Invention:

- a. Identify any related invention disclosures, patents, or other publications describing similar ideas, and other companies working in the same field. Attach copies if available.  
n/a
- b. What is the closest technology, of which you are aware?  
Standard SA-FG Flash Cell with a Photolith step to define the space between Floating Gates.
- c. Identify the advantages of this invention over previous technology.  
Reduces the total number of process steps and eliminates a Photolith step.

3.3 Important Dates:

- a. Has the invention been disclosed outside the company ☐ YES ☒ NO  
If yes, to whom, when, and in what form was the invention disclosed?
- b. Have any articles describing your invention been published? ☐ YES ☒ NO  
If yes, list author(s), title of the article, name of publication, and date?
- c. Have any engineering samples been given out? ☐ YES ☒ NO  
If yes, to whom and on what date?
- d. Has any product using the invention been sold or offered for sale?  
☐ YES ☒ NO If yes, to whom and on what date?

3.4 Disposition of the Invention:

- a. When will (or did) Micron begin use of the invention experimentally?  
Shortloops are starting in Fab4.
- b. When will (or did) Micron begin production of this invention?  
This may be used for 0.12um or 0.15um Flash.

3.5 Miscellaneous Information:

- a. Was the invention developed during a joint development agreement or other contract with an outside company? ☐ YES ☒ NO
- b. Please list developmental work outside of the company (including government proposal or contract)  
n/a.

4) **INVENTOR(S):**

Name: Kelly T. Hurley

Micron Phone: 368-5107

Mail Stop: 306

Department: Flash Process Development R&D

Dept #: 851G

Company Name (*Very Important*):

☒ Micron Technology, Inc.

☐ Micron Communications, Inc.

☐ Micron Technology (Texas)

☐ Rendition

☐ Micron Technology, Italia

☐ Micron Semiconductor Asia

☐ Other

Home Address: 3392 S. Ashbury Pl.

Boise, ID 83706

Citizenship: U.S.

Supervisor: Kirk Prall

Signature: Kelly T. Hurley

Date: 1/13/

*(all inventors must sign and date this disclosure form before it can be accepted)*

Name: Graham Wolstenholme

Micron Phone: 368-3499

Mail Stop: 306

Department: Flash Process Development R&D

Dept #: 851G

Company (Very Important):

☒ Micron Technology, Inc.

☐ Micron Communications, Inc.

☐ Micron Technology (Texas)

☐ Rendition

☐ Micron Technology, Italia

☐ Micron Semiconductor Asia

☐ Other

Home Address: 2945 East Rivernest Ct.

Boise, ID 83706

Citizenship: UK

Supervisor: Kirk Prall

Signature: G. Wolstenholme

Date: 1/13/

*(all inventors must sign and date this disclosure form before it can be accepted)*

Name: n/a

Micron Phone:

Mail Stop:

Department:

Dept #:

Company (Very Important):

- ☐ Micron Technology, Inc.  
☐ Micron Technology (Texas)  
☐ Micron Technology, Italia  
☐ Other

- ☐ Micron Communications, Inc.  
☐ Rendition  
☐ Micron Semiconductor Asia

Home Address:

Citizenship:

Supervisor:

Signature: \_\_\_\_\_ Date: \_\_\_\_\_

*(all inventors must sign and date this disclosure form before it can be accepted)*

*(for additional inventors copy the previous the page)*

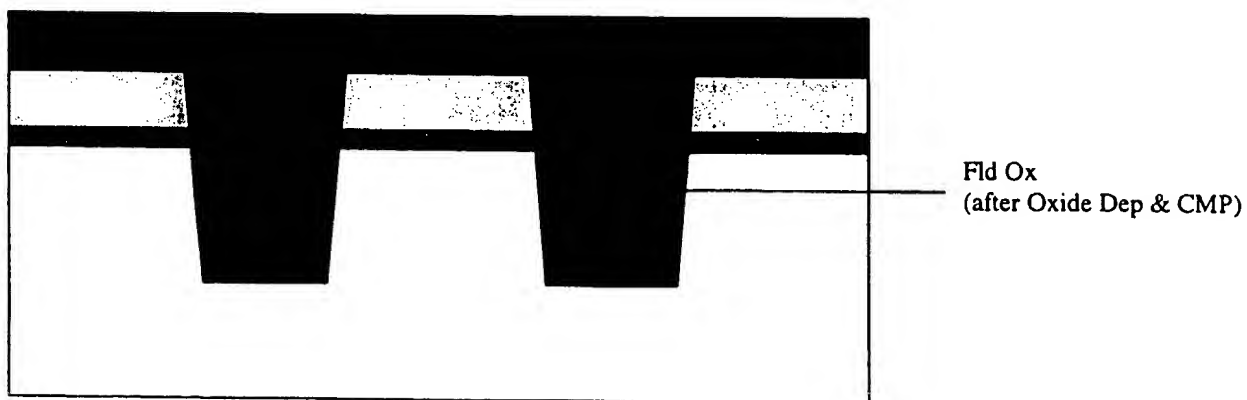
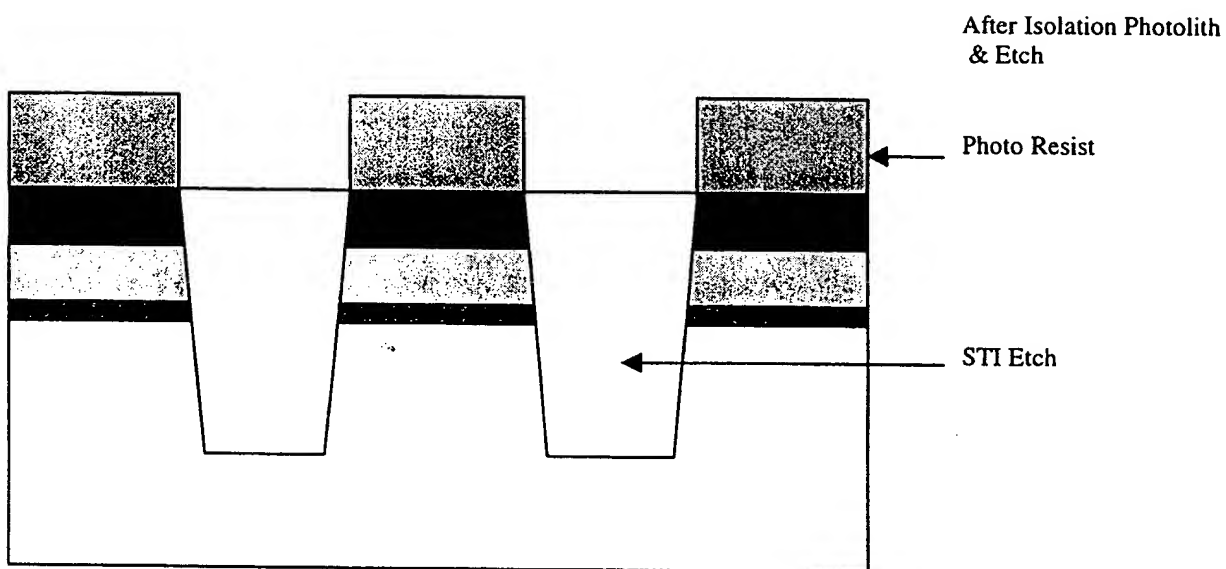
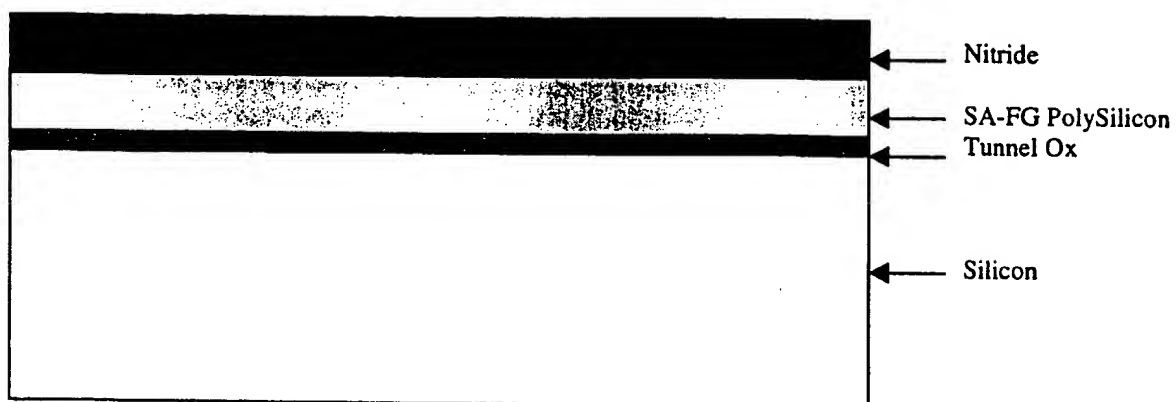
**5) WITNESS:**

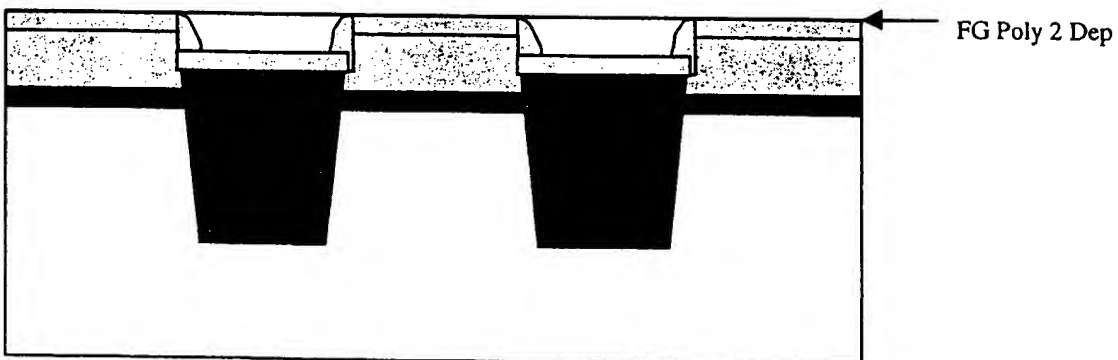
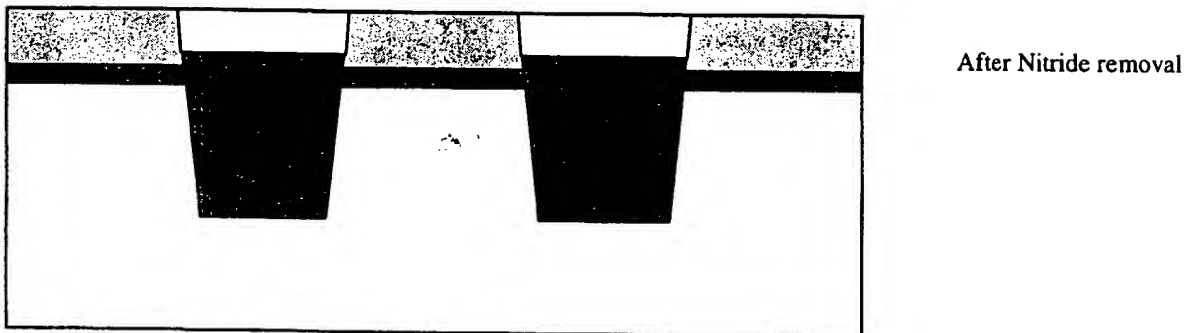
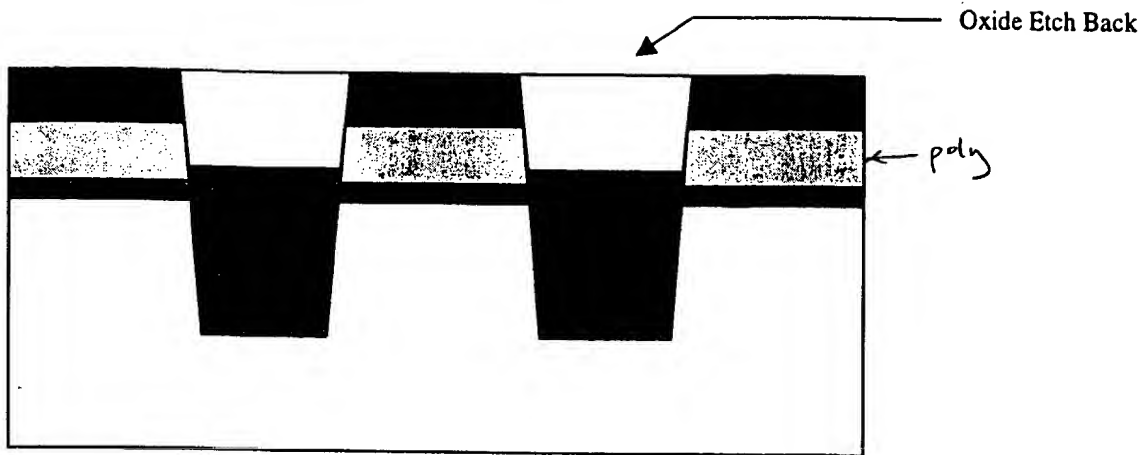
If there is only one inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

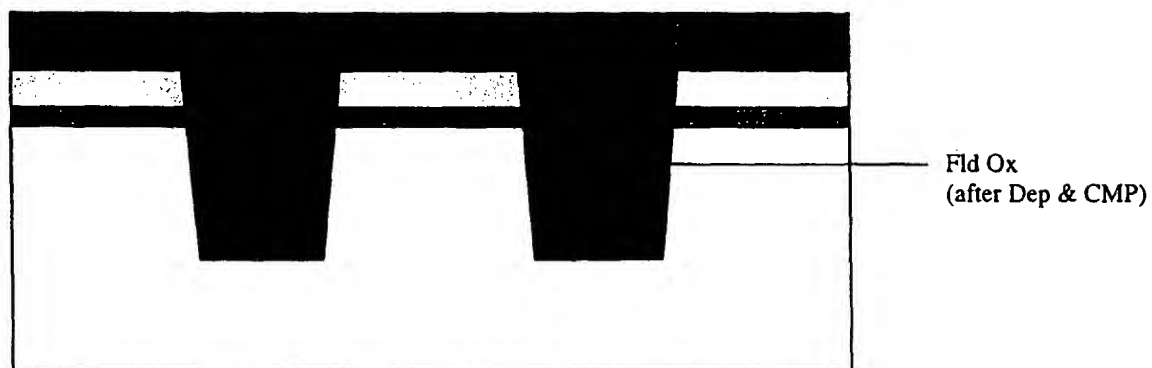
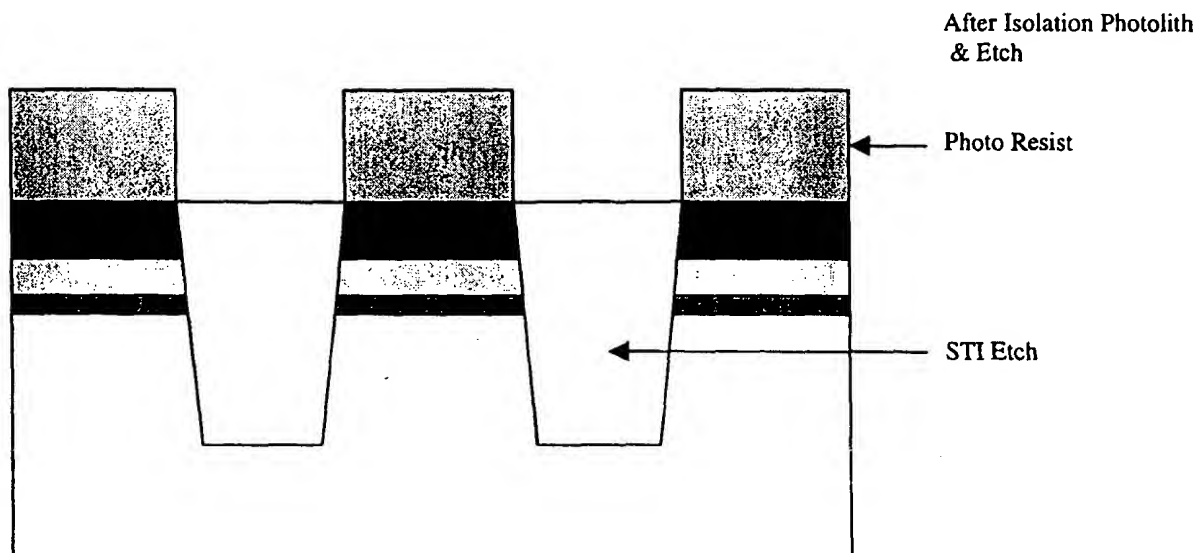
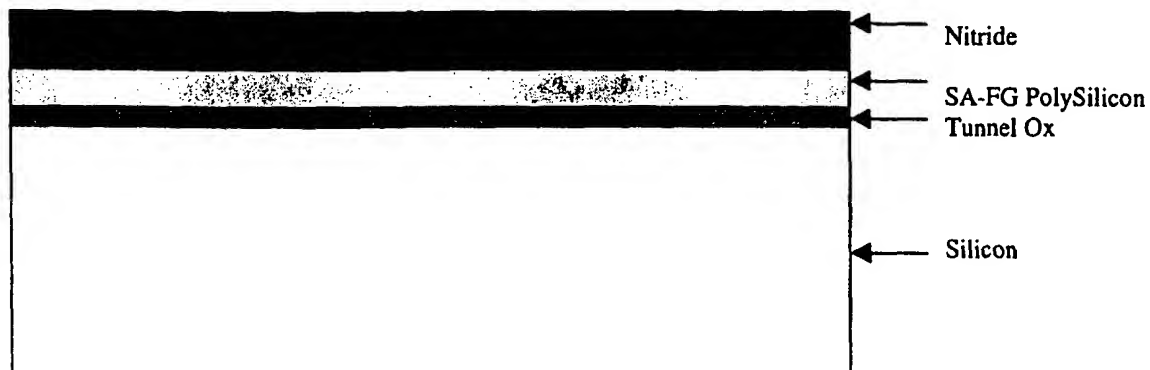
Signature: \_\_\_\_\_ Date: \_\_\_\_\_

**Note:** *If you have any questions or you need assistance completing this form, please call the Patent Department, ext. 84520.*











*Patents, Trademarks and Related Matters*  
**Killworth, Gottman, Hagan & Schaeff, L.L.P.**

One Dayton Centre  
One South Main Street, Suite 500  
Dayton, Ohio 45402-2023

937.223.2050  
Fax | 937.223.0724  
E-mail | [hghs@hghs.com](mailto:hghs@hghs.com)

October 2, 2000

**VIA FEDERAL EXPRESS**

Trish Homan-Haider  
Micron Technology, Inc.  
8000 South Federal Way  
Boise, ID 83706-9632


Re: U.S. Patent Application for **SELF-ALIGNED FLOATING  
GATE FLASH CELL SYSTEM AND METHOD**  
Our Docket MIO 0064 PA - Your Ref. 00-0028

Dear Trish:

Enclosed please find a first draft of a patent application for the above-identified Micron disclosure. Please distribute copies to the inventor(s), Graham Wolstenholme and Kelly T. Hurley. I have enclosed two additional copies (one for file and one for Patent Department review).

I understand that Messrs. Graham Wolstenholme and Kelly T. Hurley will review this draft and provide me with their comments.

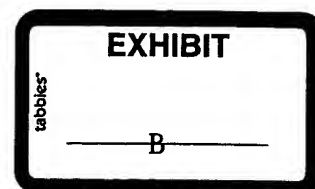
Very truly yours,

  
Gregory J. Adams  
[adamsg@kghs.com](mailto:adamsg@kghs.com)

GJA/cnb

Encls.: 4 copies of patent application and drawings

*Estimated filing fee: \$2,332.00*





NOV 15 2000

November 13, 2000

Gregory J Adams  
Killworth, Gottman, Hagan & Schaeff LLP  
One Dayton Centre  
One South Main St Suite 500  
Dayton, OH. 45402-2023

Re: Micron Docket No. 00-0028; 00-0429  
Your Reference No. MIO 0064 PA; 0065 PA

Dear Greg:

Enclosed please find the drafts for the above mentioned cases with the changes noted. Please do not hesitate to call with any questions.

Sincerely,

A handwritten signature in cursive script, appearing to read "Susan", is written over the typed name.

Susan Sweesy  
Patent Assistant

Phone: (208) 368-4596  
Fax: (208) 368-5606  
FedEx Ref No. 823138407163

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**Killworth, Gottman, Hagan & Schaeff, LLP**

One Dayton Centre  
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937.223.2050  
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E-mail | [kghs@kghs.com](mailto:kghs@kghs.com)

**VIA FEDERAL EXPRESS**

December 18, 2000

Susan Sweesy  
Micron Technology, Inc.  
8000 S. Federal Way  
P O Box 6  
Boise, ID 83706-0006

Re: U.S. Patent Application entitled **SELF-ALIGNED FLOATING GATE FLASH CELL  
SYSTEM AND METHOD** - Our Docket MIO 0064PA; Your Ref. 00-0028

Dear Susan:

Enclosed is a revised draft of a patent application for the above identified Micron disclosure. This draft has been revised according to the comments we received regarding the first draft. We have not received comments specifically from the inventors and we do not know if they had approved the previous draft. Therefore, we are including formal papers with this draft in the event that there are no further comments.

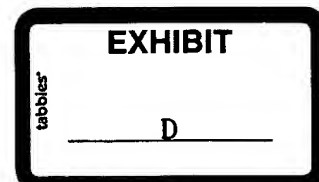
Please note that we did not include means-plus function claims in the present application because the structure of the present invention does not lend itself to a definition in terms of its function.

If you have any questions regarding this matter, please do not hesitate to contact me.

Very truly yours,

Gregory J. Adams  
[adamsg@kghs.com](mailto:adamsg@kghs.com)

GJA/AMS  
Encl.





Micron Technology, Inc.  
8000 South Federal Way  
P.O. Box 6  
Boise, Idaho 83707-0006

Date 3-13-01

Number of pages including cover sheet \_\_\_\_\_

To: Melody Sullivan  
Gregory Adams  
Killworth, et. al

From: Trish Homan-Haider

Patent Department8000 S. Federal Way,  
M/S 525Boise, ID 83716Phone 937-223-2050Phone (208) 368-4518Fax Phone 937-223-0724Fax Phone (208) 368-5606

CC: \_\_\_\_\_

CC: \_\_\_\_\_

## REMARKS:

☒ Urgent☒ For your review☒ Reply ASAP☐ Please comment

## Comments:

Sheq, here are some chgs for the inventor -  
It had one more thing to say, so I didn't  
get it Fed-Ex'd.

## Confidentiality Notice:

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Attorney Docket No.:  
MIO 0064 PA /00-0028

*Photo Resist would be removed  
before Field Oxide is deposited. 4/5/01  
3/7/01*

chemical mechanical planarization (CMP) could be used as one type of mechanical planarization. The photo resist 505 is also removed. Figure 5C illustrates the stacked gate region at this stage of the method.

5 An oxide etch back is performed at block 408 to remove a determined amount of the field oxide 507 so that the field oxide 507 is below an upper surface of the FG poly layer 503. *and above the upper surface of 502* Figure 5D illustrates the stacked gate region after the oxide etch back has been performed. The nitride layer 504 is removed at block 10 409. The nitride layer 504 can be removed by a process such as etching. Figure 5E illustrates the stacked gate region after the nitride layer 504 has been removed. *see 3/7/01*

After the nitride layer 504 has been removed, a second polysilicon layer 508 is deposited over the stacked gate region at block 410. The second polysilicon layer 508 may also be 15 referred to as FG poly 2. Figure 5F illustrates the stacked gate region at this stage of the method.

A spacer etch is performed to remove portions of the second poly layer 508 at block 411 leaving the floating gate poly wings 20 509 of figure 5G. A spacer etch is a method of selectively etching.

Other conventional steps of processing may be performed on the stacked gate region such as, oxide nitride oxide (ONO)